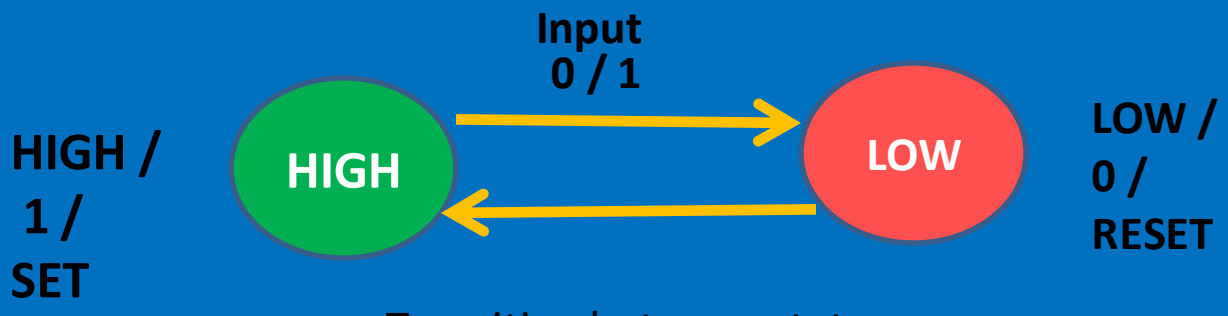
FLIP FLOPS

Binary unit capable of storing one bit – 0 or 1

Flip Flop has two stable states and a transition between these two states .

Transition is depended on input.



Transition between states

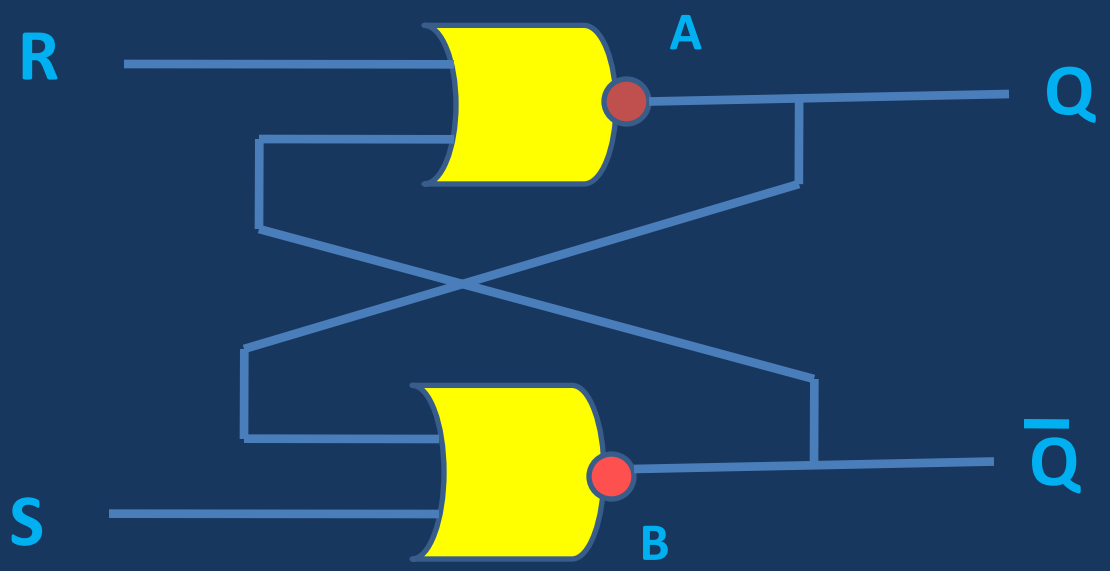
Types of FLIP FLOPS

RS - FLIP FLOP

Block Diagram

RS - FLIP FLOP

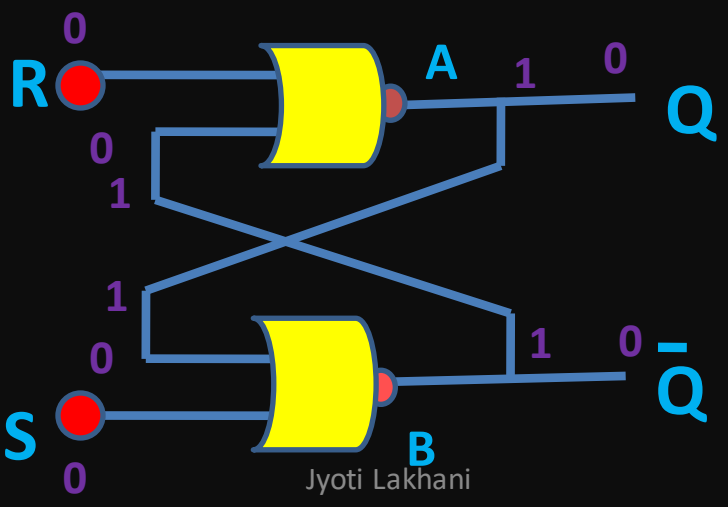
RS Latch using NOR Gate



RS - FLIP FLOP

TRUTH TABLE

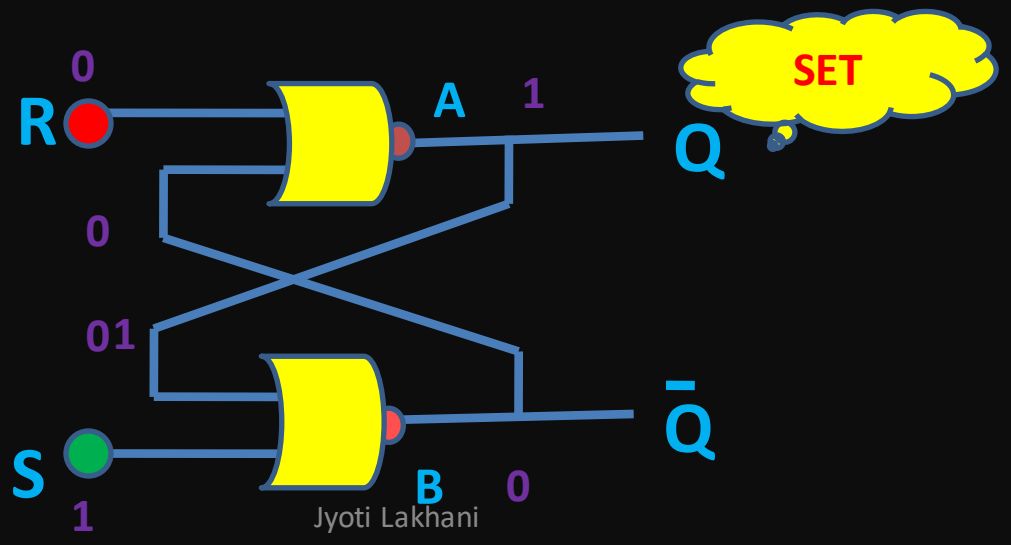
	R	S	Q
Case 1	0	0	NC
Case 2	0	1	SET
Case 3	1	0	RESET
Case 4	1	1	*



RS - FLIP FLOP

TRUTH TABLE

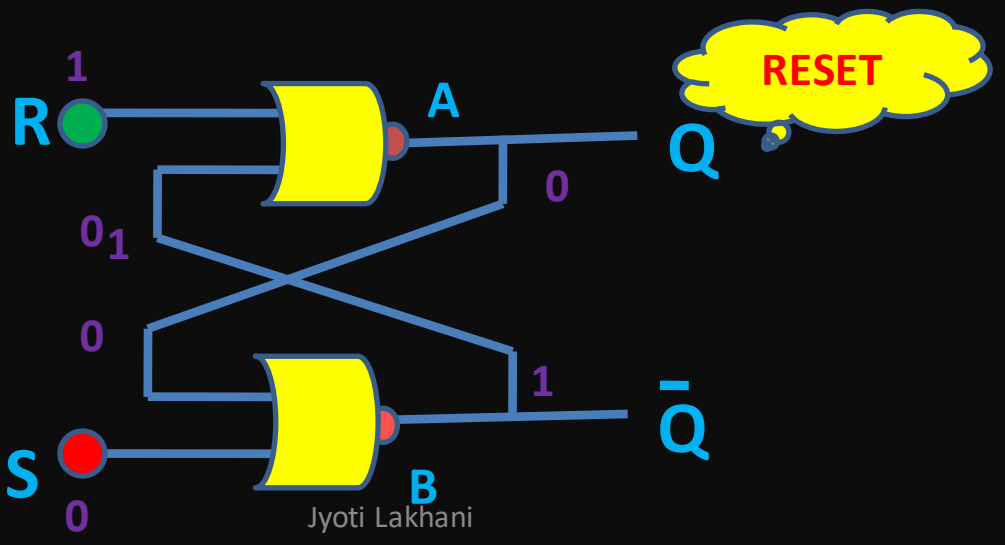
	R	S	Q
Case 1	0	0	NC
Case 2	0	1	SET
Case 3	1	0	RESET
Case 4	1	1	*



RS - FLIP FLOP

TRUTH TABLE

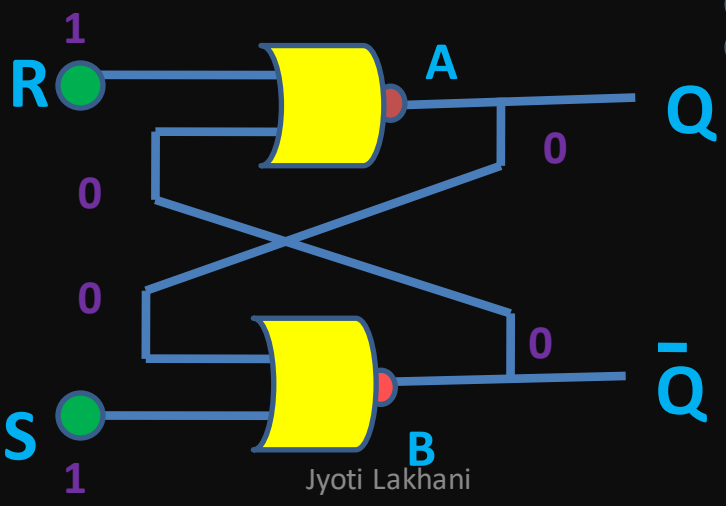
	R	S	Q
Case 1	0	0	NC
Case 2	0	1	SET
Case 3	1	0	RESET
Case 4	1	1	*



RS - FLIP FLOP

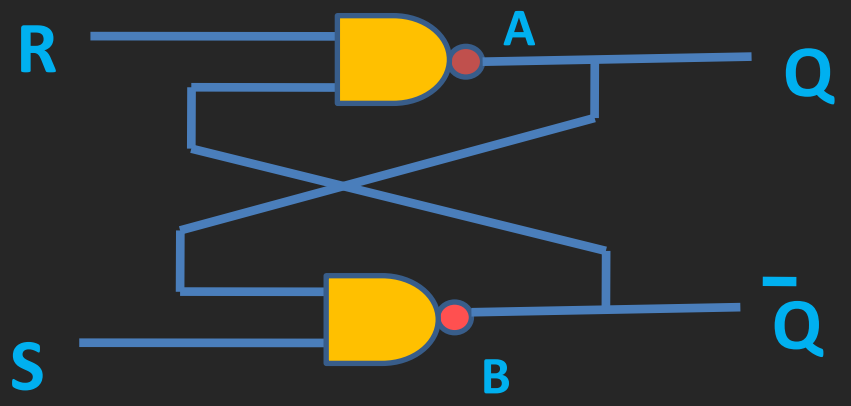
TRUTH TABLE

	R	S	Q
Case 1	0	0	NC
Case 2	0	1	SET
Case 3	1	0	RESET
Case 4	1	1	*



$\bar{R}\bar{S}$ - FLIP FLOP

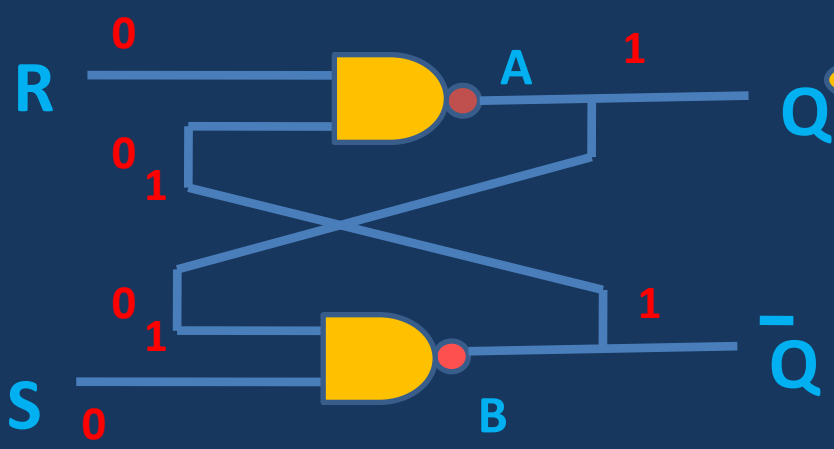
RS Latch using NAND Gate ($\bar{R}\bar{S}$ Flip Flop)



$\bar{R}$	$\bar{S}$	Q
0	0	*
0	1	SET
1	0	RESET
1	1	NC

$\bar{R}\bar{S}$ - FLIP FLOP

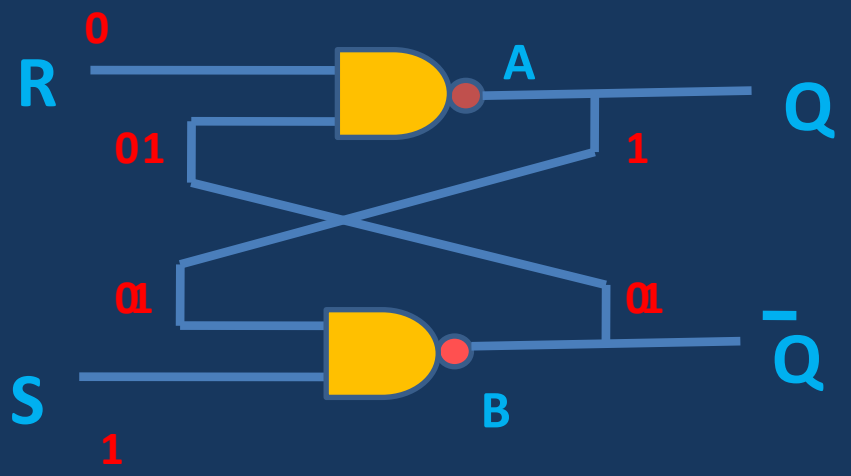
RS Latch using NAND Gate



$\bar{R}$	$\bar{S}$	Q
0	0	*
0	1	SET
1	0	RESET
1	1	NC

$\bar{R}\bar{S}$ - FLIP FLOP

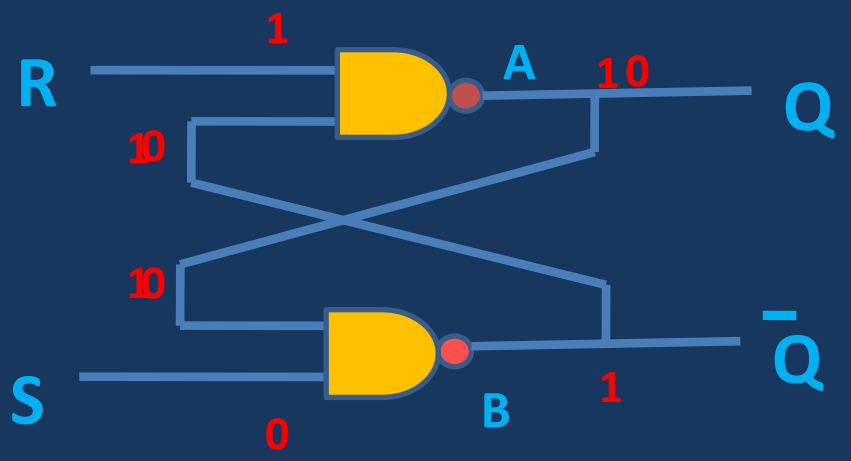
RS Latch using NAND Gate ($\bar{R}\bar{S}$ Flip Flop)



$\bar{R}$	$\bar{S}$	Q
0	0	*
0	1	SET
1	0	RESET
1	1	NC

$\bar{R}\bar{S}$ - FLIP FLOP

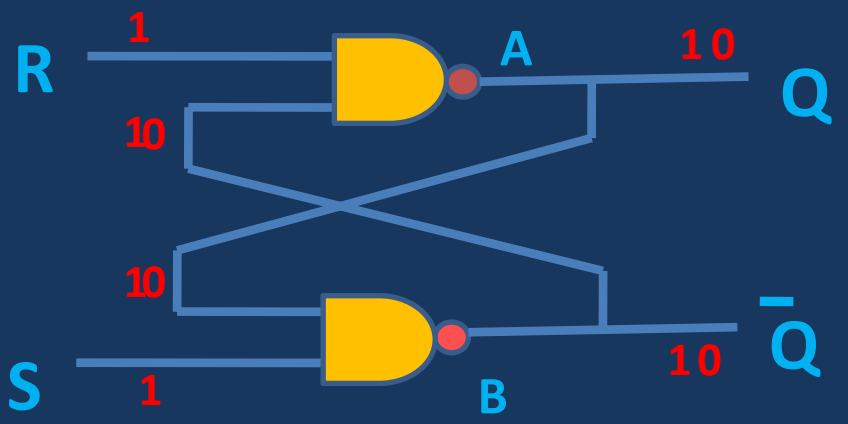
RS Latch using NAND Gate



$\bar{R}$	$\bar{S}$	Q
0	0	*
0	1	SET
1	0	RESET
1	1	NC

$\bar{R}\bar{S}$ - FLIP FLOP

RS Latch using NAND Gate



$\bar{R}$	$\bar{S}$	Q
0	0	*
0	1	SET
1	0	RESET
1	1	NC

Clocked RS Flip Flop

What is the Difference ????

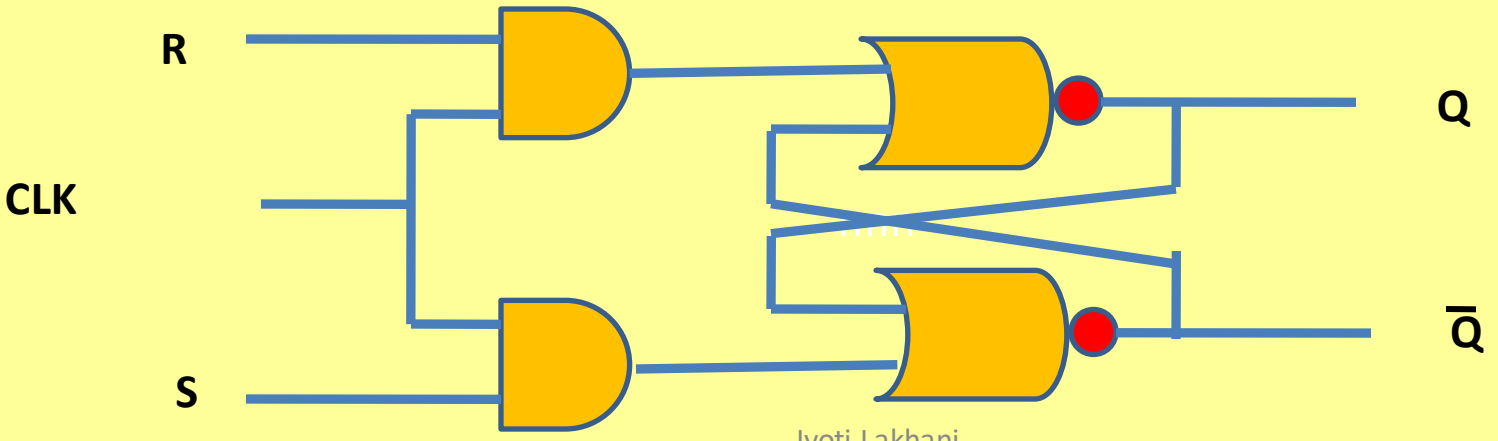
A Clock signal is added to the input

What Clock Signal will do ????

Clock Signal controls the instant at which flip flop changes the state

How to Design ???

Basic NOR- Flip Flop + Two AND Gates + A Clock Signal



Clocked RS Flip Flop

Block Diagram of Clocked RS Flip Flop

Rule of RS Flip Flop : $\bar{Q}$ is always complement of Q

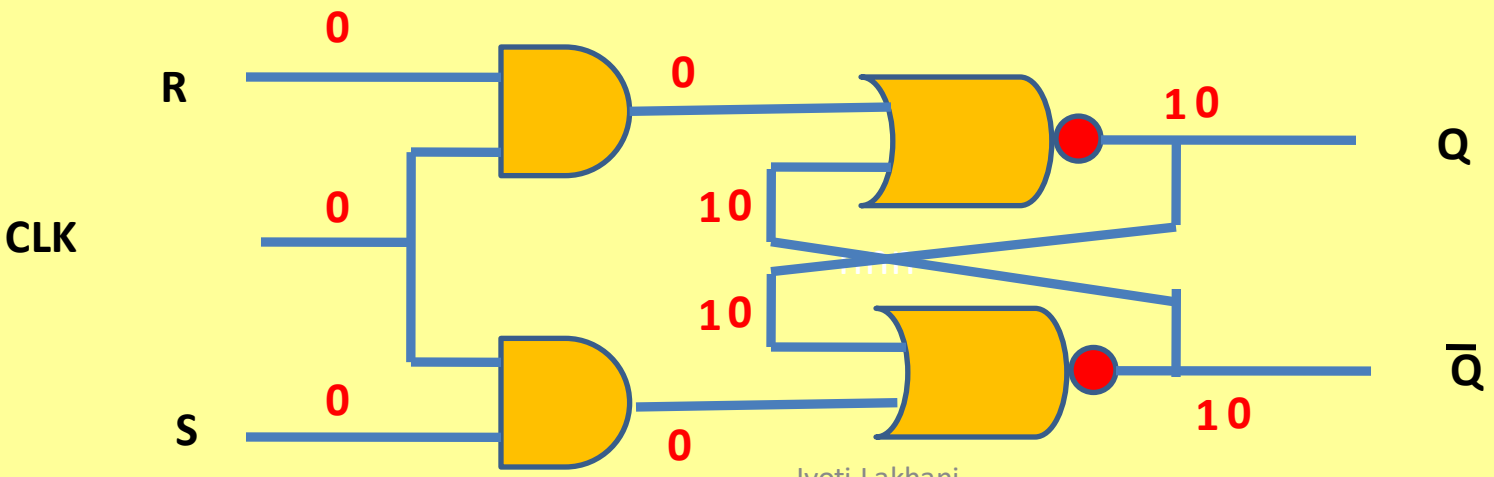
TRUTH TABLE

R	S	CLK	Qn	Qn+1	ACTION	Case
0	0	0	0	0	NC	1
			1	1	NC	2
		1	0	0	NC	3
			1	1	NC	4
0	1	0	0	0	NC	5
			1	1	NC	6
		1	0	1	SET	7
			1	1	SET	8
1	0	0	0	0	NC	9
			1	1	NC	10
		1	0	0	RESET	11
			1	0	RESET	12
1	1	0	0	0	NC	13
			1	1	NC	14
		1	0	?	ERROR	15
			1	?	ERROR	16

Clocked RS Flip Flop

Case 1

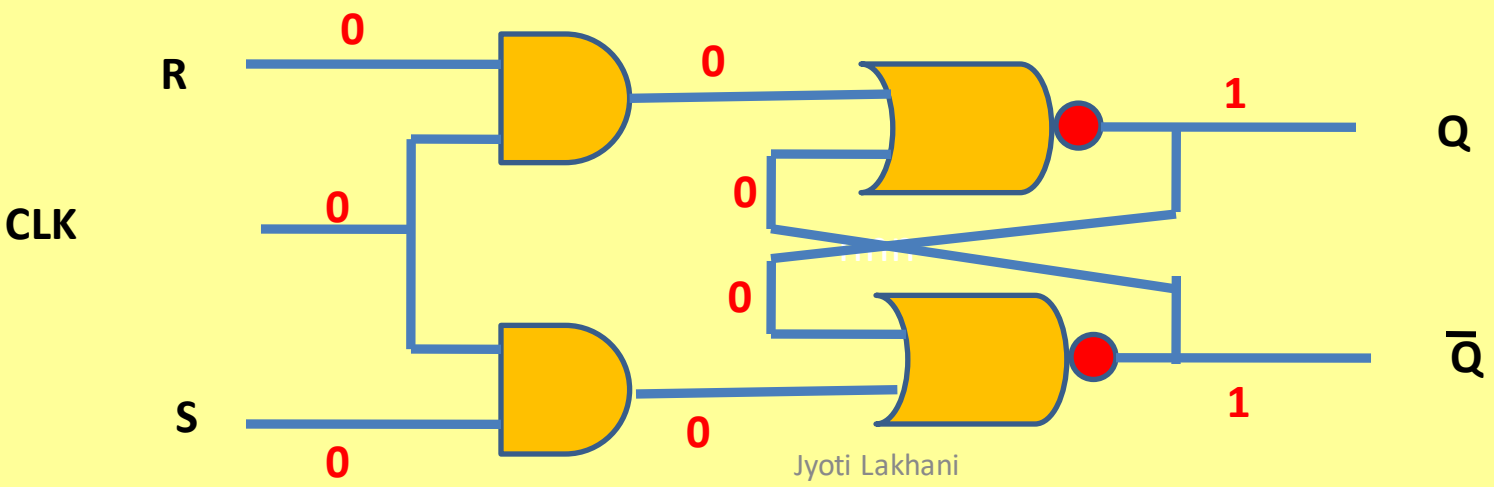
R	S	CLK	Qn	Qn+1	ACTION
0	0	0	0	0	NC



Clocked RS Flip Flop

Case 2

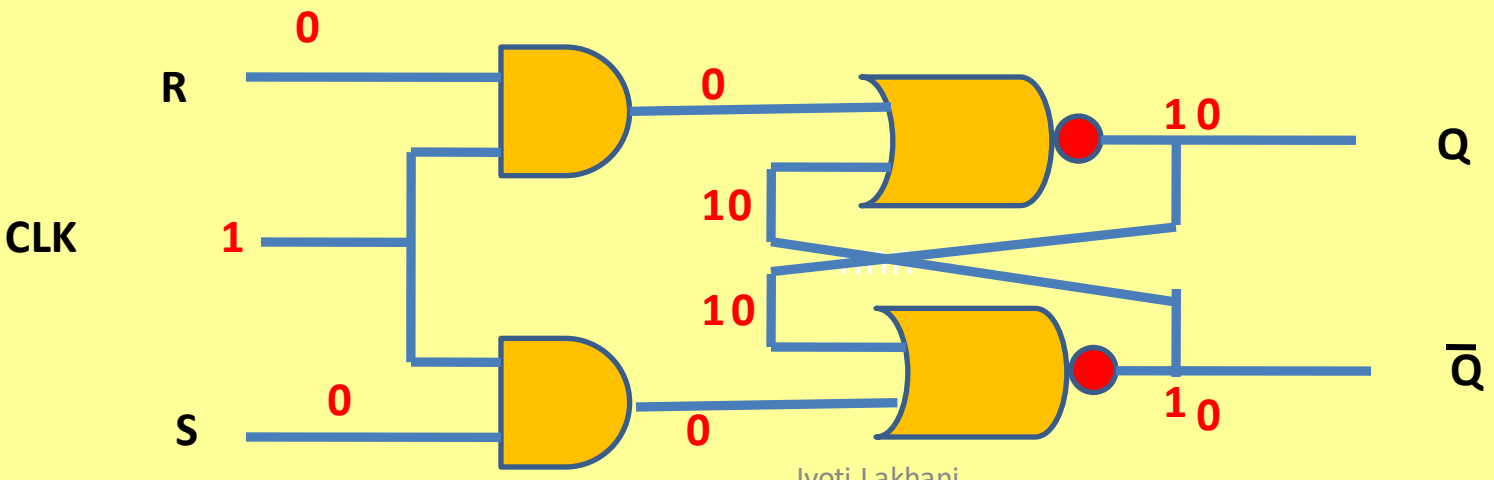
R	S	CLK	Qn	Qn+1	ACTION
0	0	0	1	1	NC



Clocked RS Flip Flop

Case 3

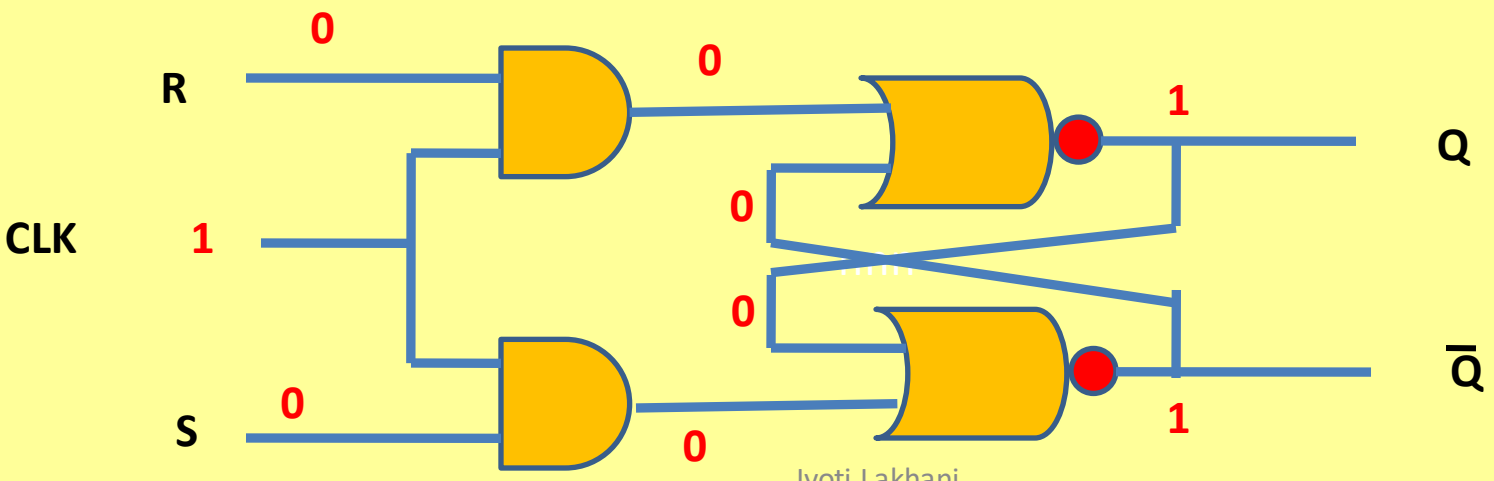
R	S	CLK	Qn	Qn+1	ACTION
0	0	1	0	0	NC



Clocked RS Flip Flop

Case 4

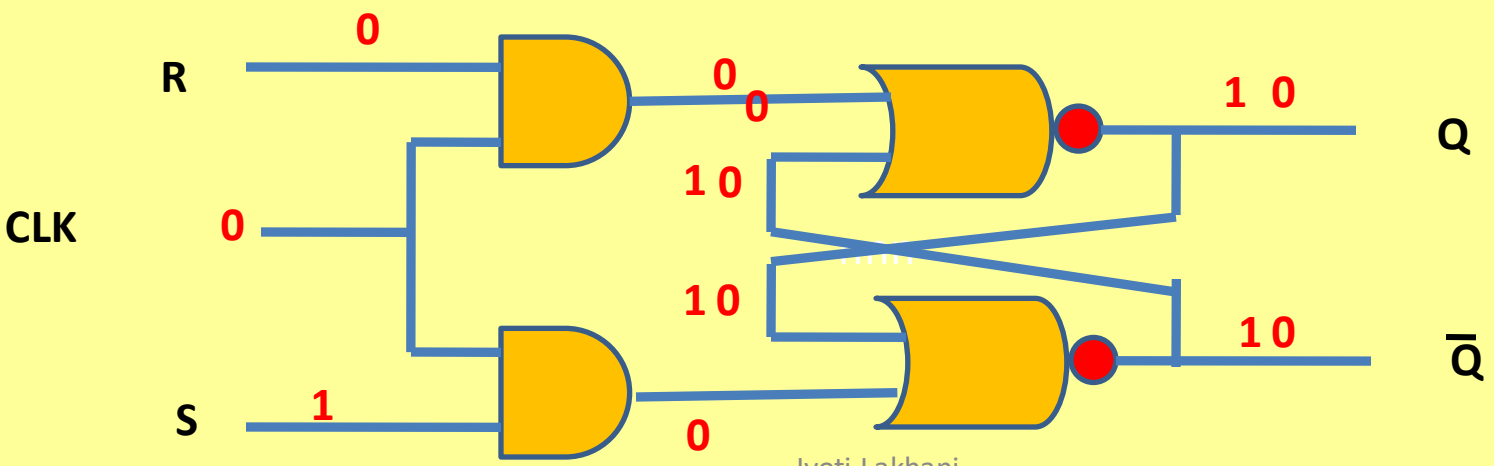
R	S	CLK	Qn	Qn+1	ACTION
0	0	1	1	1	NC



Clocked RS Flip Flop

Case 5

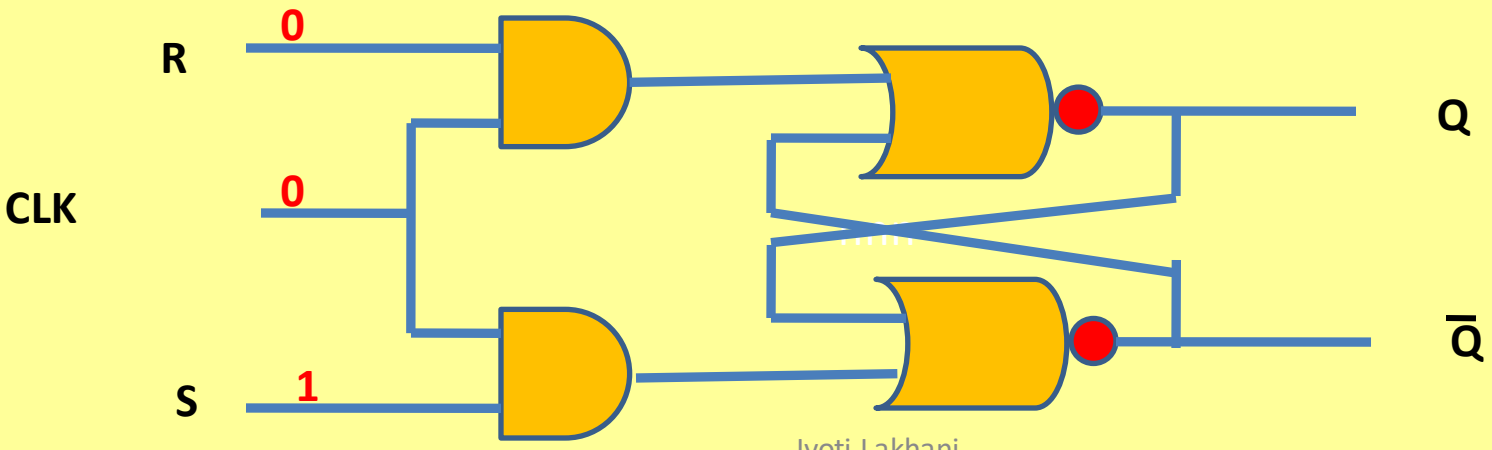
R	S	CLK	Qn	Qn+1	ACTION
0	1	0	0	0	NC



Clocked RS Flip Flop

Case 6

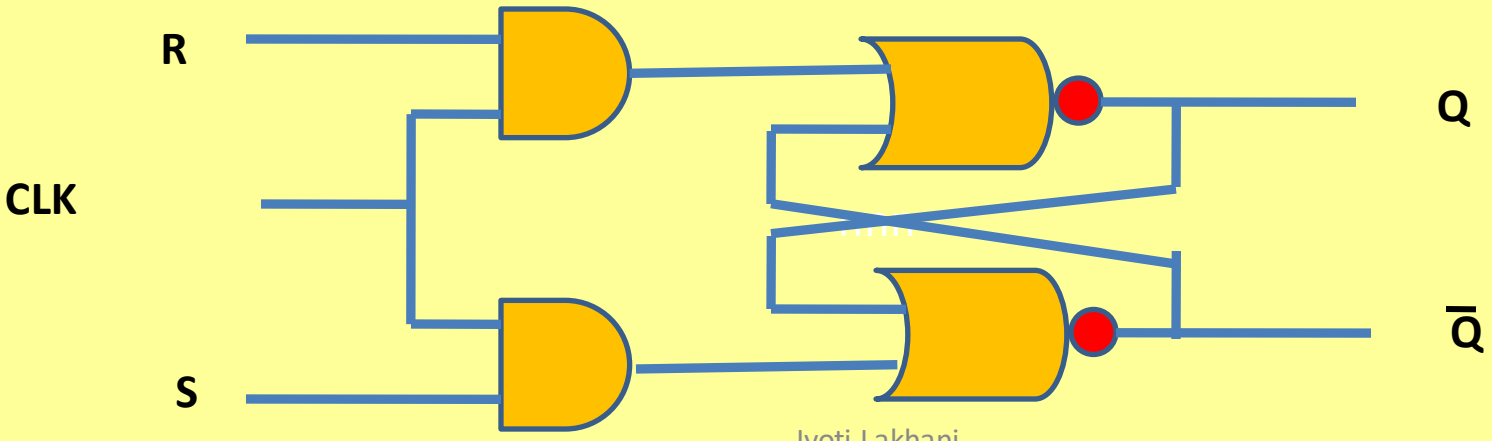
R	S	CLK	Qn	Qn+1	ACTION
0	1	0	1	1	NC



Clocked RS Flip Flop

Case 7

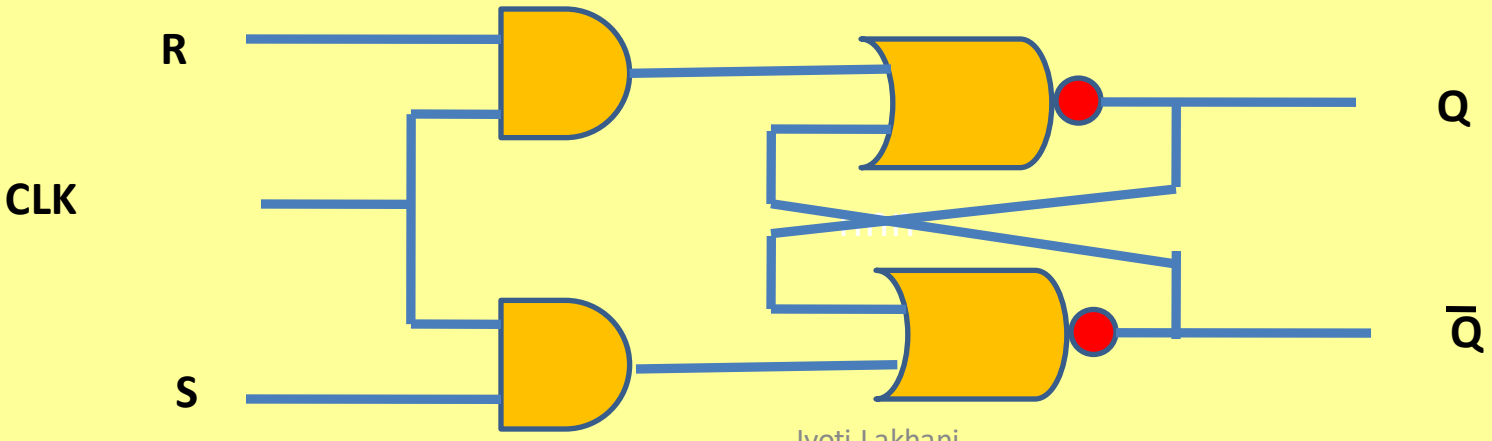
R	S	CLK	Qn	Qn+1	ACTION
0	1	1	0	1	SET



Clocked RS Flip Flop

Case 8

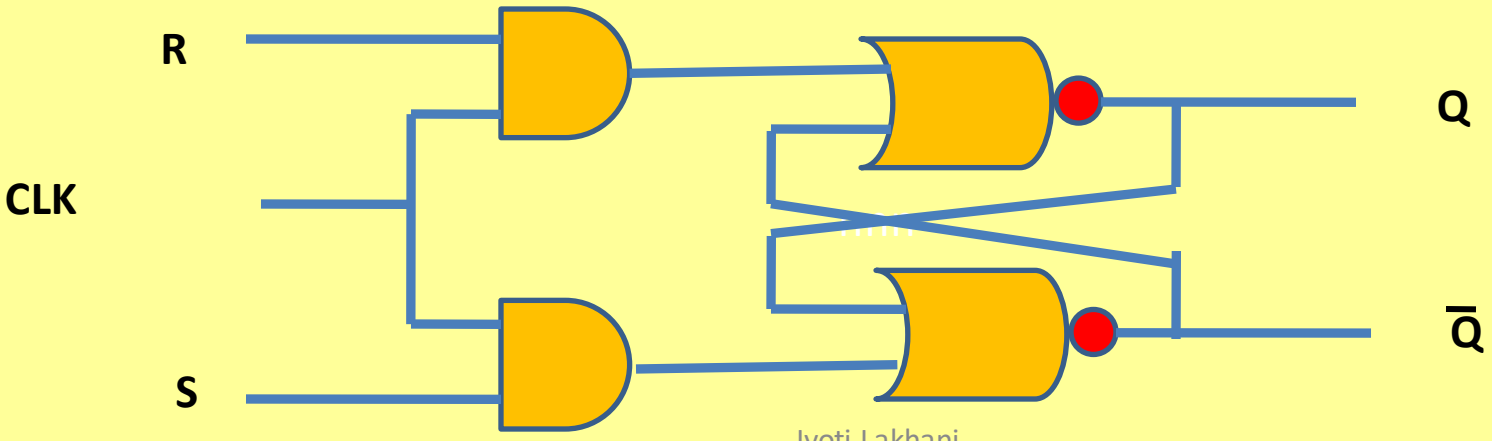
R	S	CLK	Qn	Qn+1	ACTION
0	1	1	1	1	SET



Clocked RS Flip Flop

Case 9

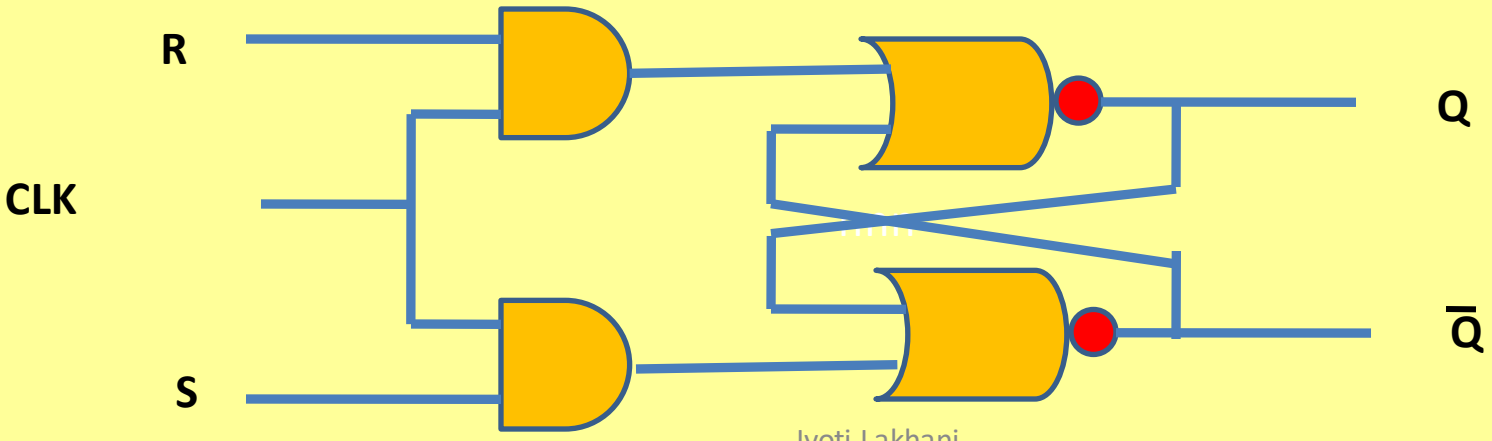
R	S	CLK	Qn	Qn+1	ACTION
1	0	0	0	0	NC



Clocked RS Flip Flop

Case 10

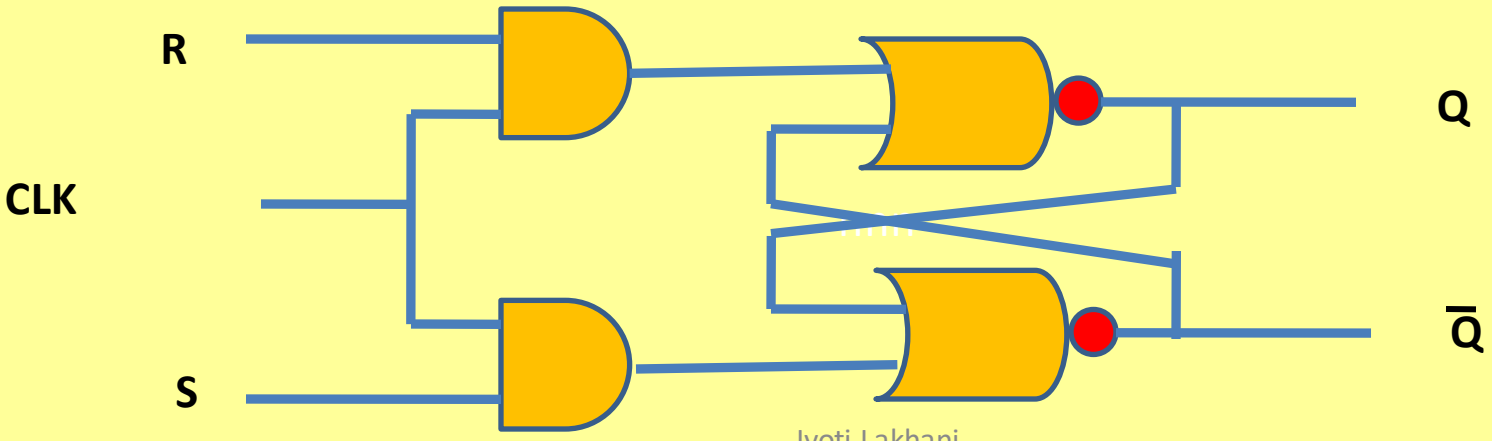
R	S	CLK	Qn	Qn+1	ACTION
1	0	0	1	1	NC



Clocked RS Flip Flop

Case 11

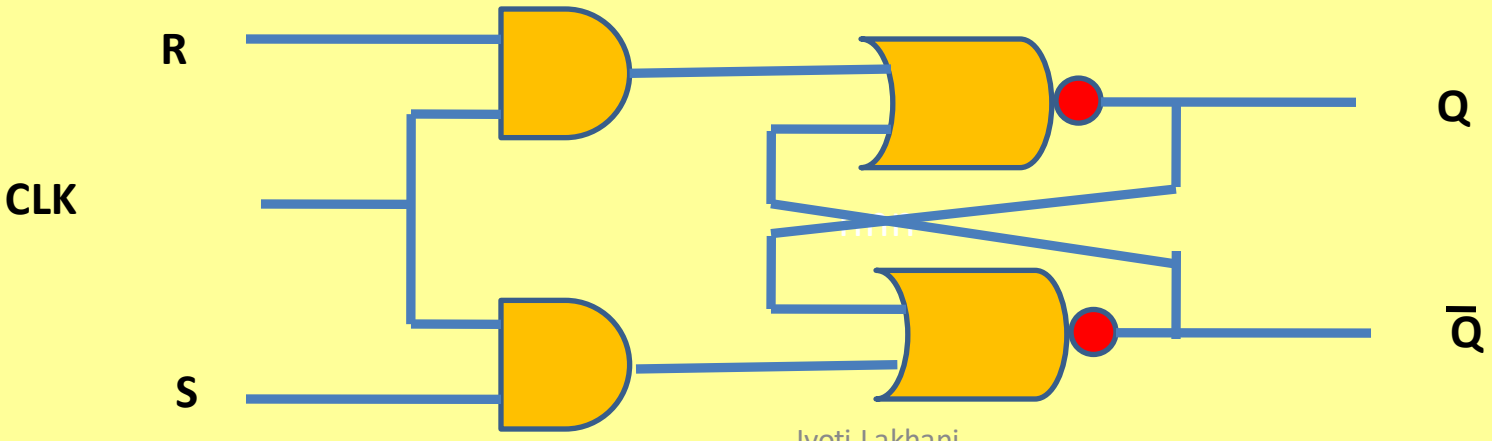
R	S	CLK	Qn	Qn+1	ACTION
1	0	1	0	0	RESET



Clocked RS Flip Flop

Case 12

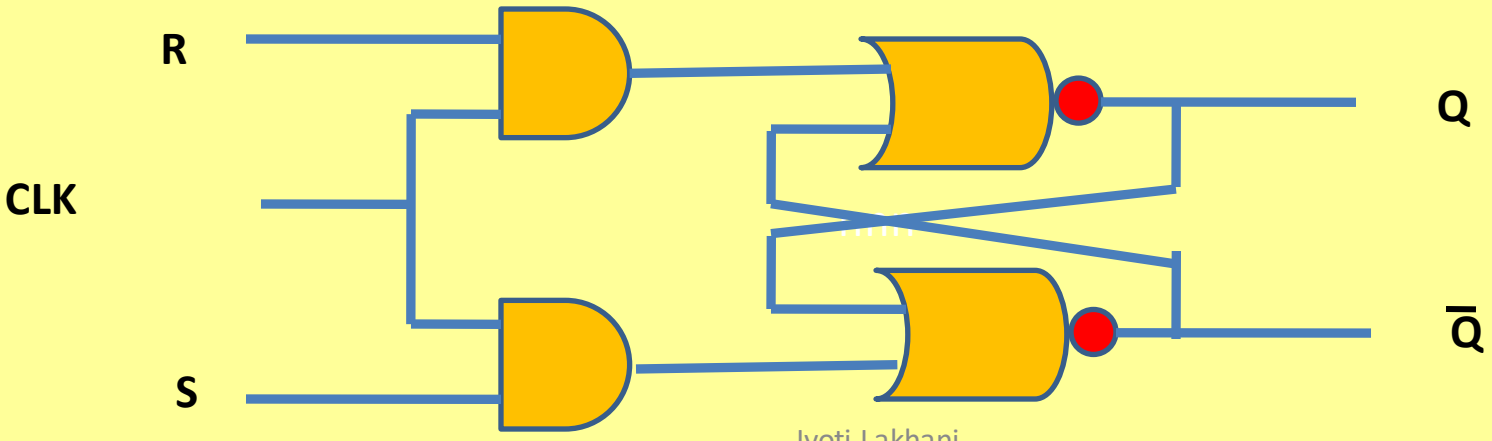
R	S	CLK	Qn	Qn+1	ACTION
1	0	1	1	0	RESET



Clocked RS Flip Flop

Case 13

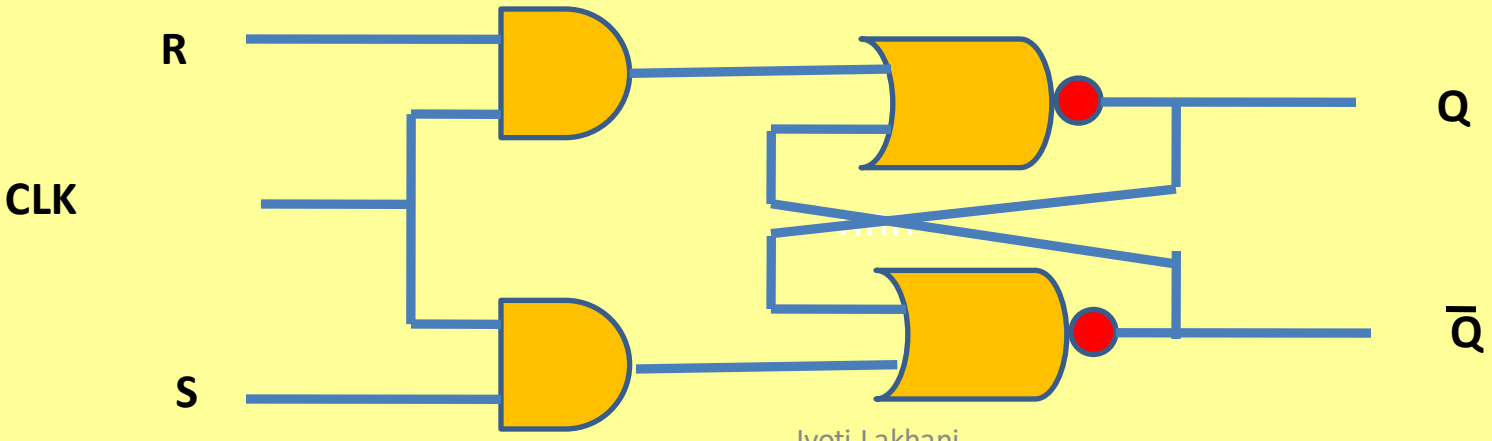
R	S	CLK	Qn	Qn+1	ACTION
1	1	0	0	0	NC



Clocked RS Flip Flop

Case 14

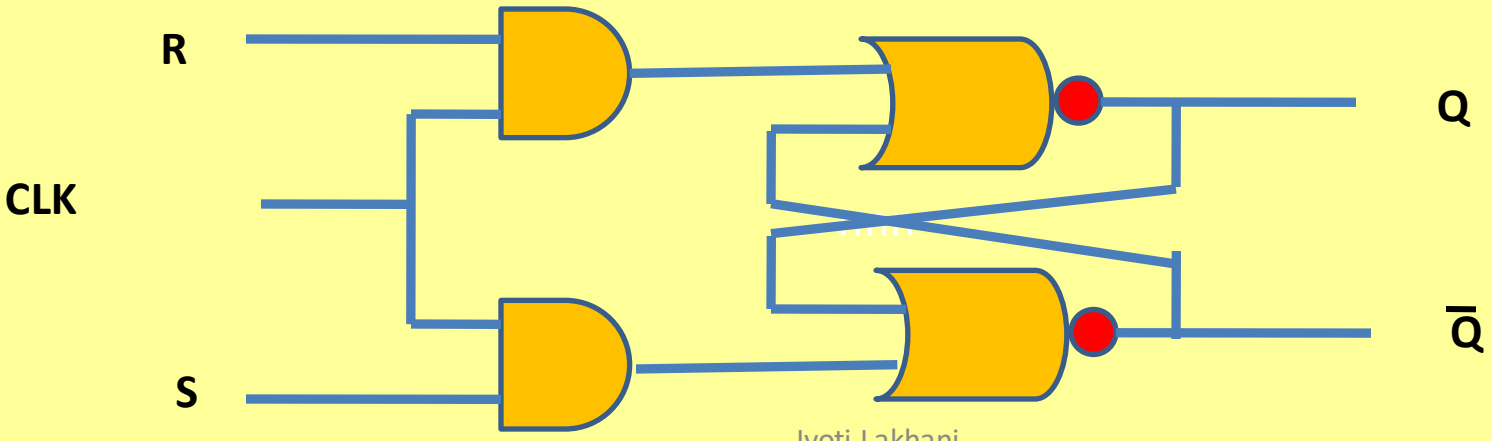
R	S	CLK	Qn	Qn+1	ACTION
1	1	0	1	1	NC



Clocked RS Flip Flop

Case 15

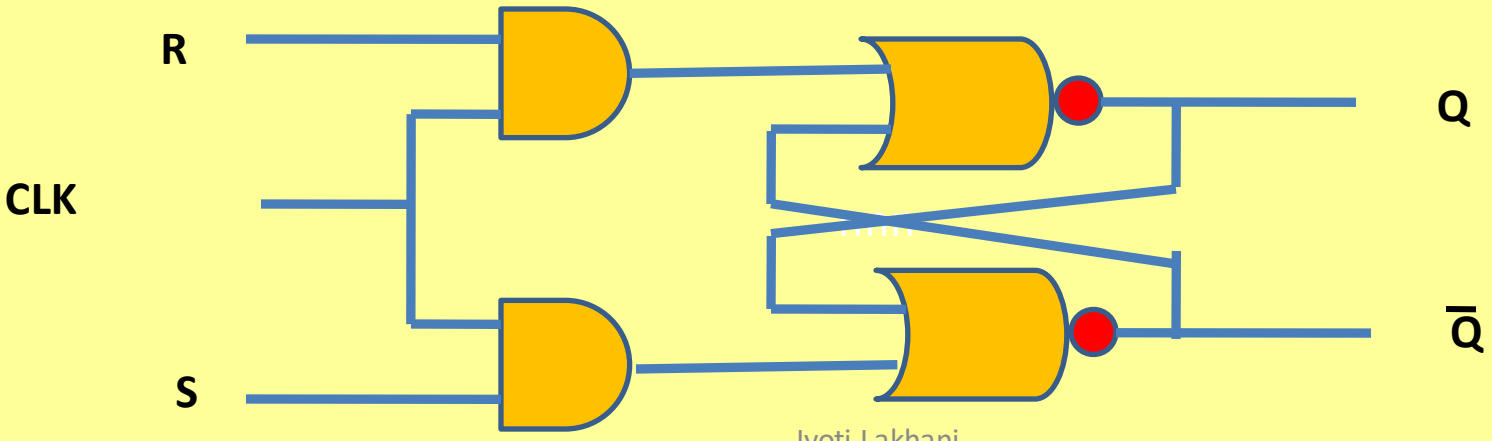
R	S	CLK	Qn	Qn+1	ACTION
1	1	1	0	?	ERROR



Clocked RS Flip Flop

Case 16

R	S	CLK	Qn	Qn+1	ACTION
1	1	1	1	?	ERROR



D – Flip Flop (Delay Flip Flop) (Clocked)

1. Stores digital info
2. Has Single input
3. It does not have Race Condition

D Flip Flop = One RS Latch + One Inverter

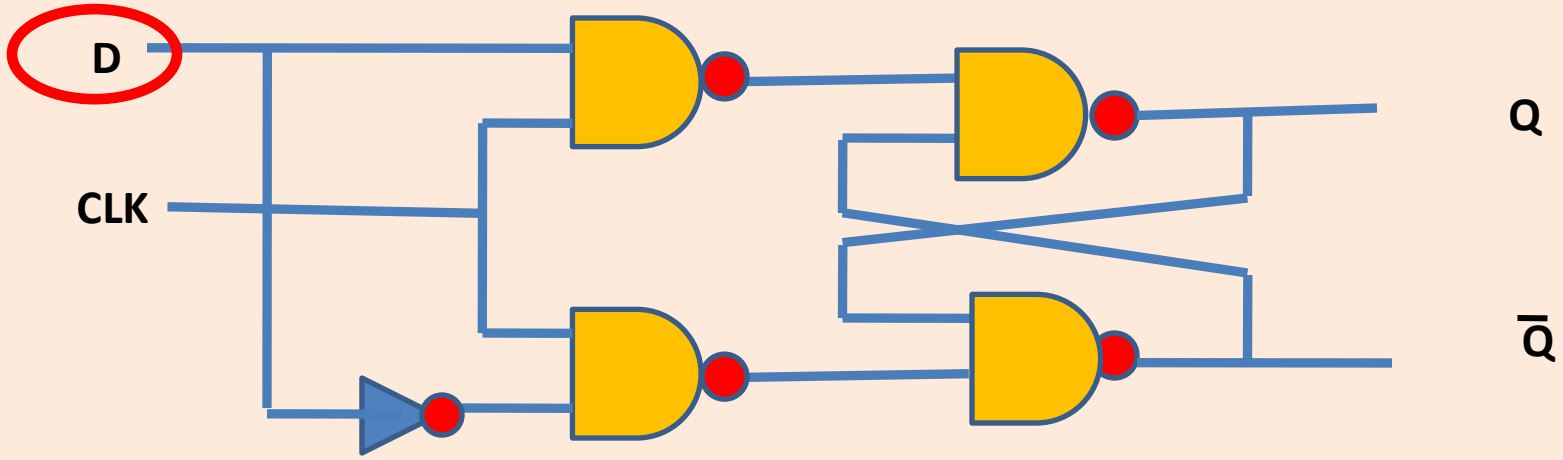
D – Flip Flop (Delay Flip Flop) (Clocked)

D Flip Flop using NAND Gate

When Clock is LOW : AND gates of Flip Flop are ENABLE

When Clock is HIGH : AND gates of Flip Flop are DISABLE

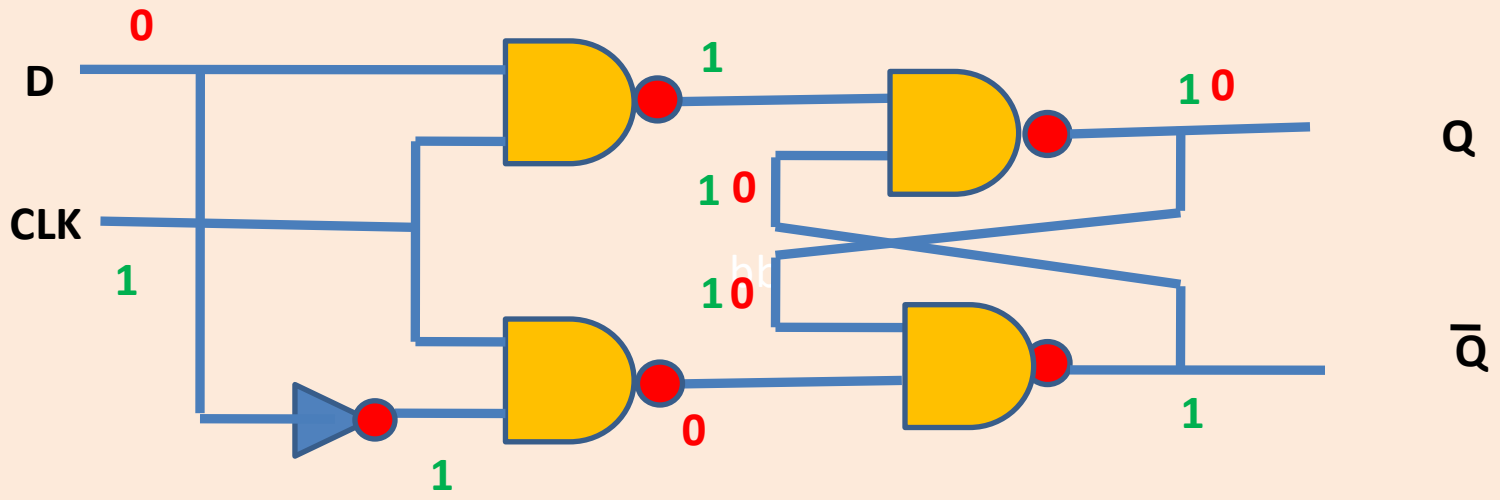
Single Input



D – Flip Flop (Delay Flip Flop) (Clocked)

Truth Table

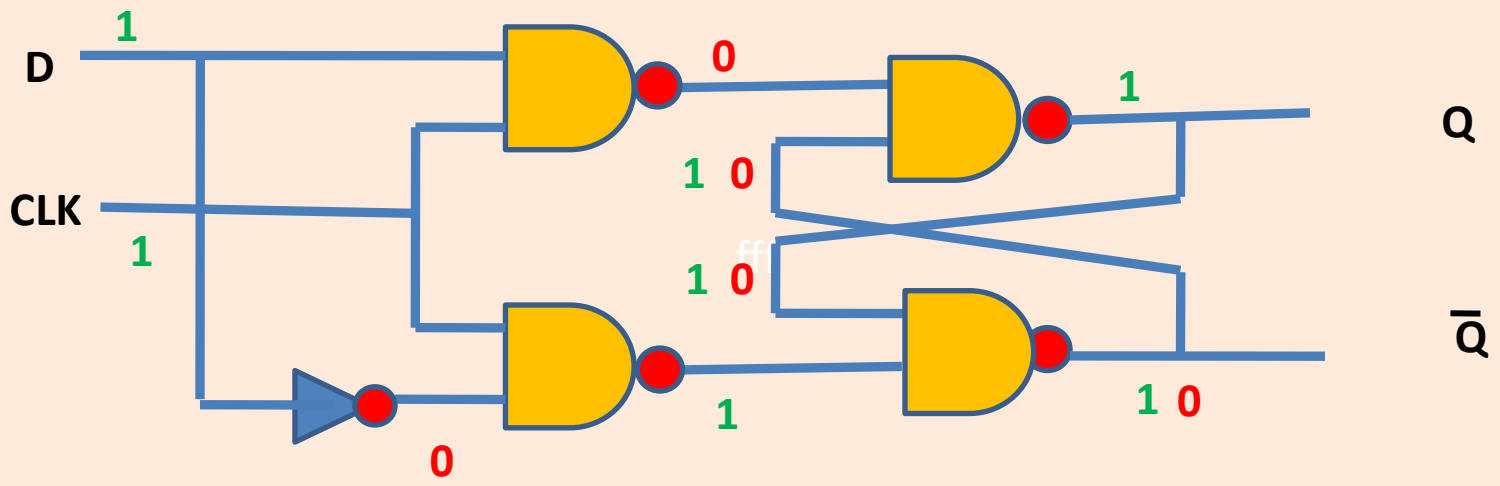
Clock	Input (D)	Output (Q)
1	0	0
1	1	1
0	x	No Change



D – Flip Flop (Delay Flip Flop) (Clocked)

Truth Table

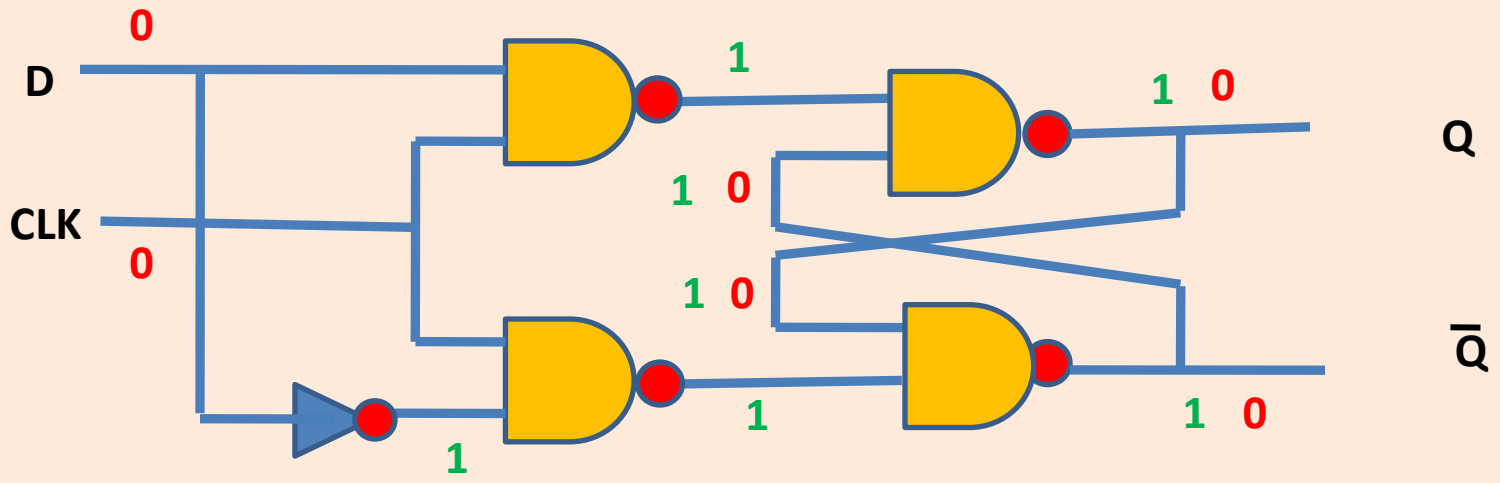
Clock	Input (D)	Output (Q)
1	0	0
1	1	1
0	x	No Change



D – Flip Flop (Delay Flip Flop) (Clocked)

Truth Table

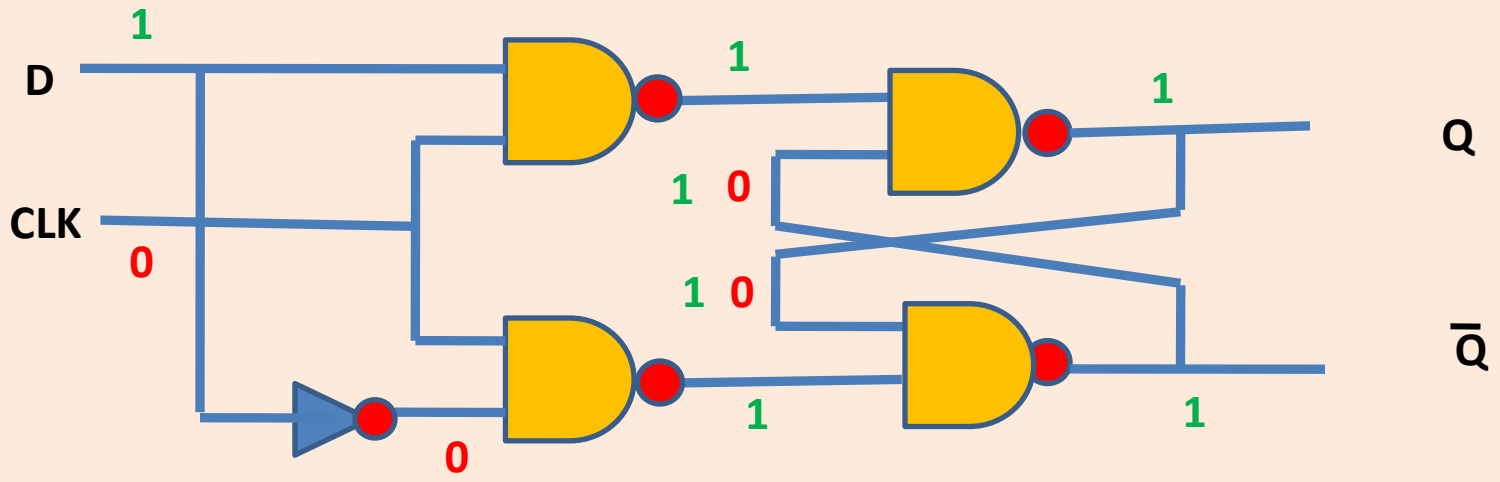
Clock	Input (D)	Output (Q)
1	0	0
1	1	1
0	x	No Change



D – Flip Flop (Delay Flip Flop) (Clocked)

Truth Table

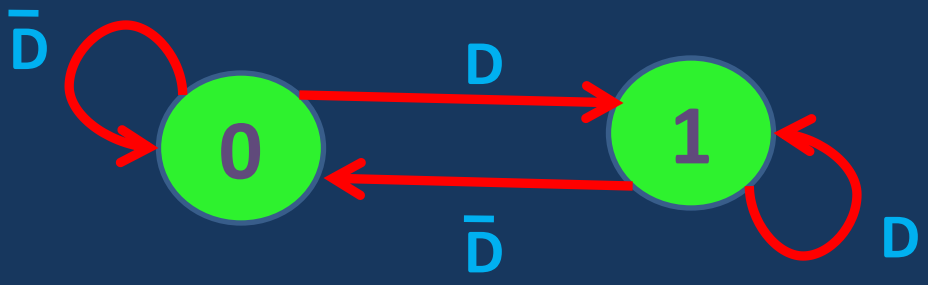
Clock	Input (D)	Output (Q)
1	0	0
1	1	1
0	x	No Change



D – Flip Flop (Delay Flip Flop) (Clocked)

State Transition Diagram

Q (t)	D	Q (t+1)
0	0	0
0	1	1
1	0	0
1	1	1



JK Flip Flop

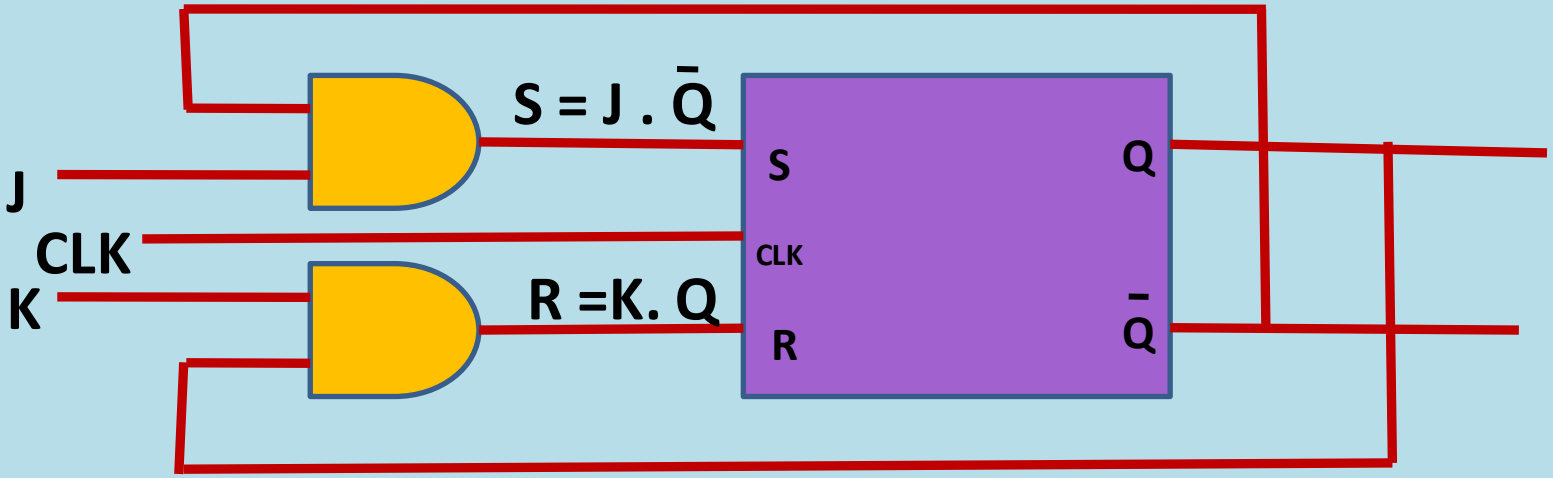
- Similar to SR Flip Flop
- Input J and K behaves like SET and RESET

When J = K = 1, the Flip Flop Output Toggles

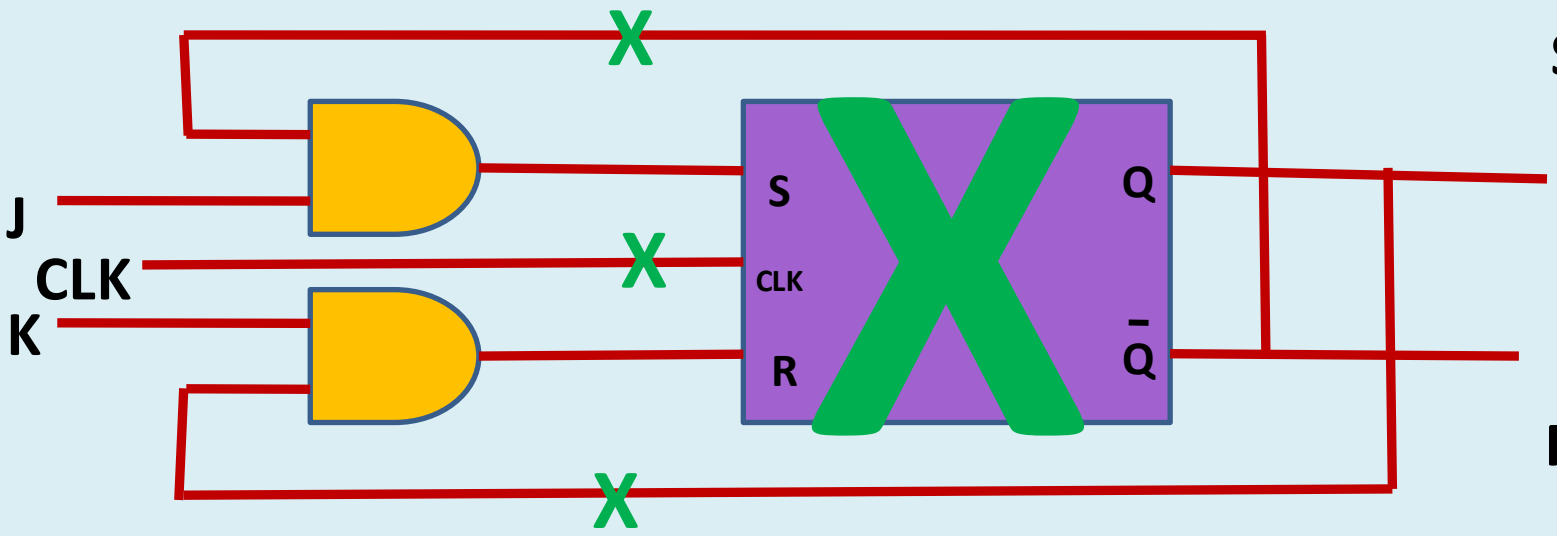
If Q = 0, it switches to 1

if Q = 1, it switches to 0

JK Flip Flop using SR Flip Flop

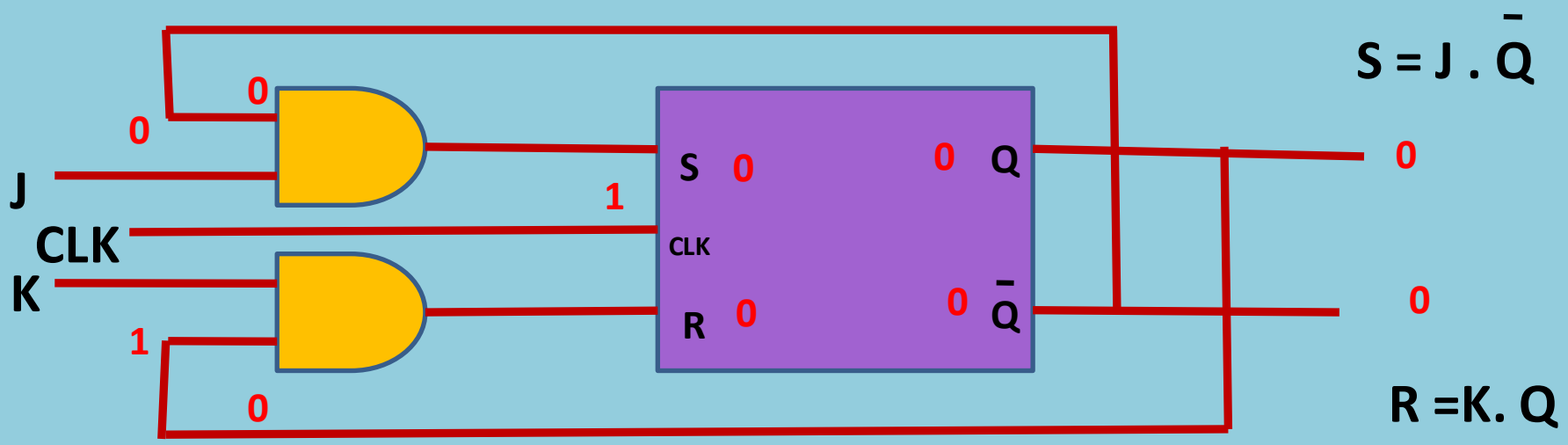


JK Flip Flop



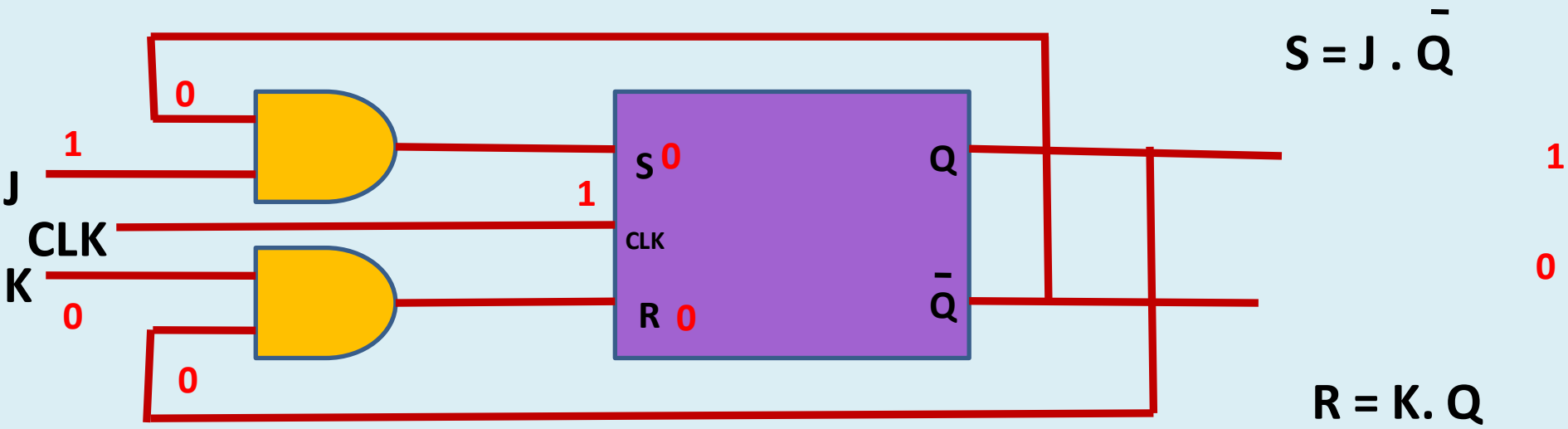
Clock	Inputs		Output Qn+1	Action
	J	K		
X	0	0	Qn	NC
1	0	1	0	RESET
1	1	0	1	SET
1	1	1	Qn	TOGGLE

JK Flip Flop



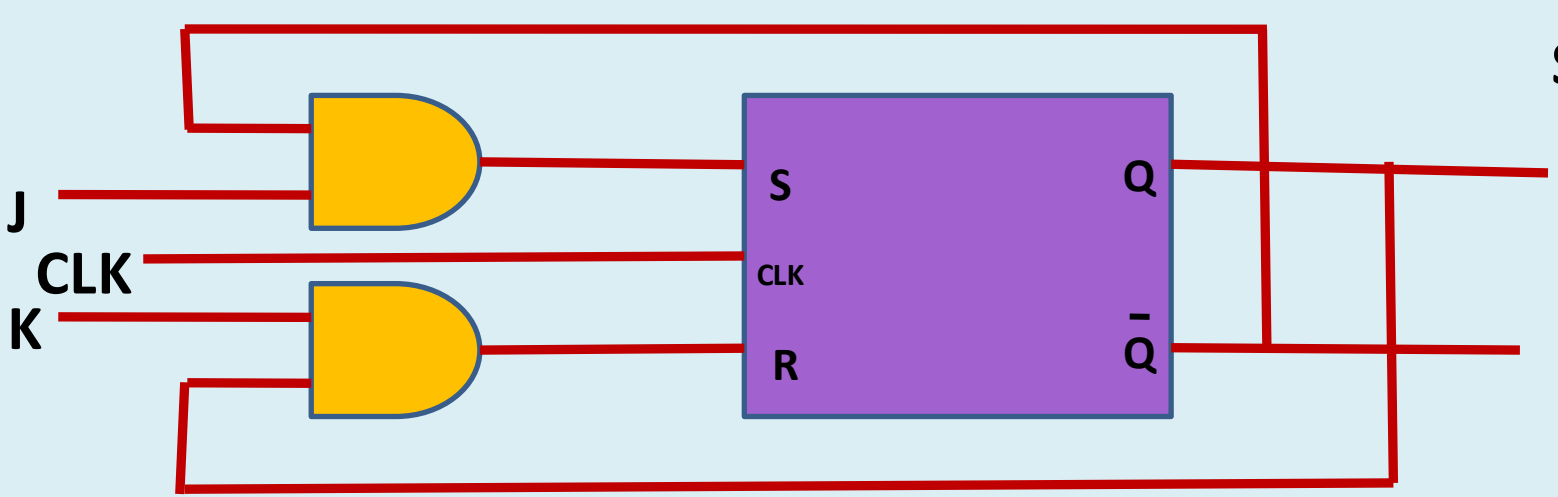
Clock	Inputs		Output Qn+1	Action
	J	K		
X	0	0	Qn	NC
1	0	1	0	RESET
1	1	0	1	SET
1	1	1	Qn	TOGGLE

JK Flip Flop



Clock	Inputs		Output Qn+1	Action
	J	K		
X	0	0	Qn	NC
1	0	1	0	RESET
1	1	0	1	SET
1	1	1	Qn	TOGGLE

JK Flip Flop



$S = J \cdot \bar{Q}$

$R = K \cdot Q$

Clock	Inputs		Output Qn+1	Action
	J	K		
X	0	0	Qn	NC
1	0	1	0	RESET
1	1	0	1	SET
1	1	1	Qn	TOGGLE